# Beyond the  of the next generation IoT RF transceivers

## Dutch RF Conference

Kees van Nieuwburg - November 29, 2017

ItoM

# Meet Kees van Nieuwburg


- Born in Den Bosch
- Married, 2 children
- 3D-Printing, Cooking, Sports

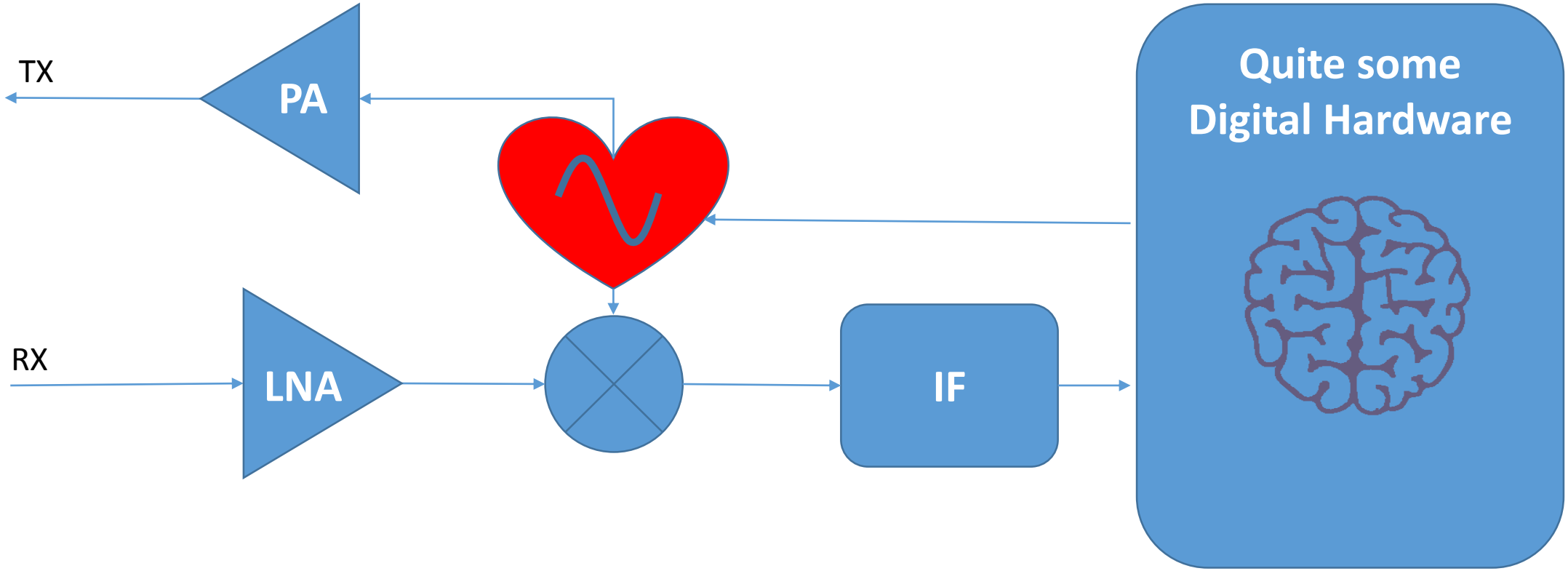
- 12 years at ItoM
- Transceivers, Signal processing algorithms, ..

# Outline

- Introduction
- Design Challenges
- Some of the Opportunities
- Future Vision

# Introduction | Next Generation RF Transceivers

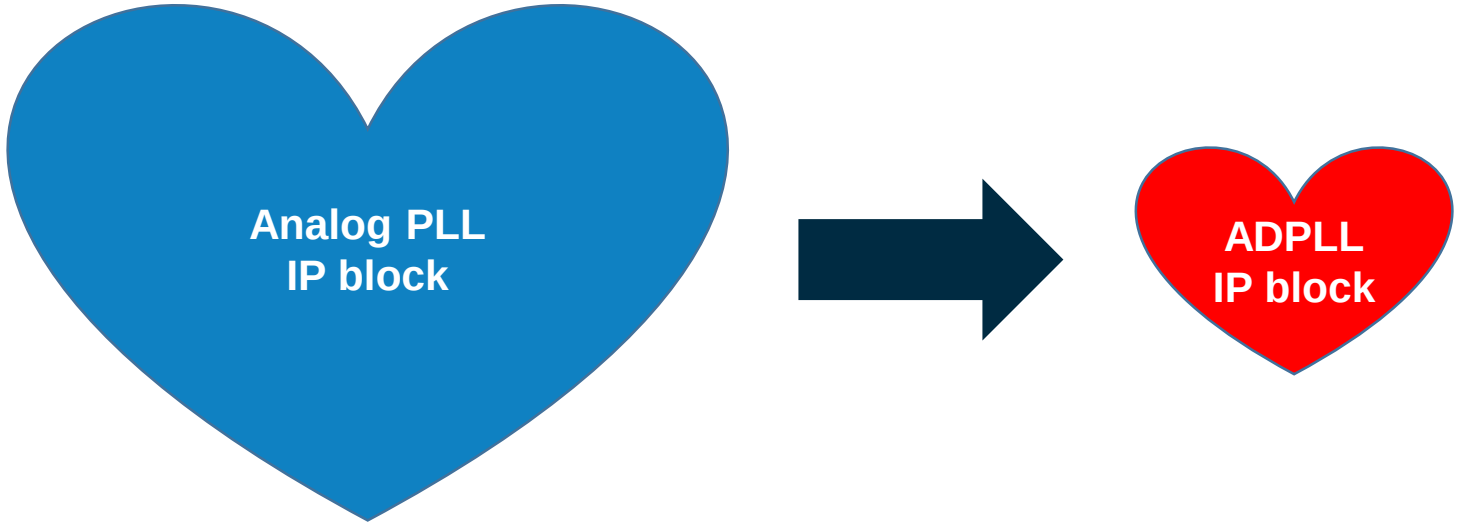
## PLL is the heart of every modern RF Transceiver



# Introduction | Next RF Transceiver Generations

## ADPLL IP block offers huge advantages for RF Transceivers

- Drastically reduce die size and decrease power consumption
- Increase of flexibility & performance
- Increase robustness of the system
- More future proof for future process technologies

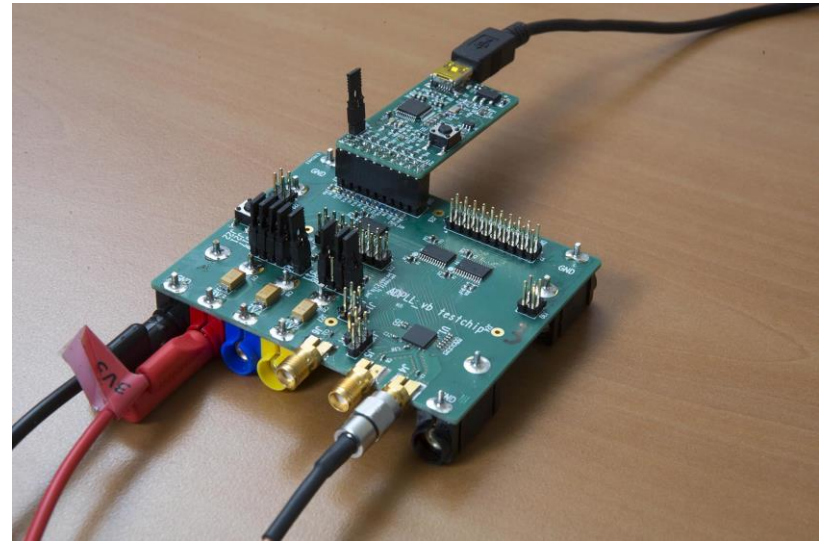


# Introduction | A family of ADPLL IP blocks

**Low current ADPLL for Bluetooth Low Energy**

- Power consumption 1.2mA in 55nm CMOS
- Area 0.12mm$^2$, including LDOs (area reduction factor 4)

√validated silicon



**Low current ADPLL for Audio communication**

- Power consumption 15mA in 55nm CMOS
- Area 0.5mm$^2$, including LDOs
- Modulation FSK up to D8PSK, more performance, bit rate 3Mbps

√validated silicon

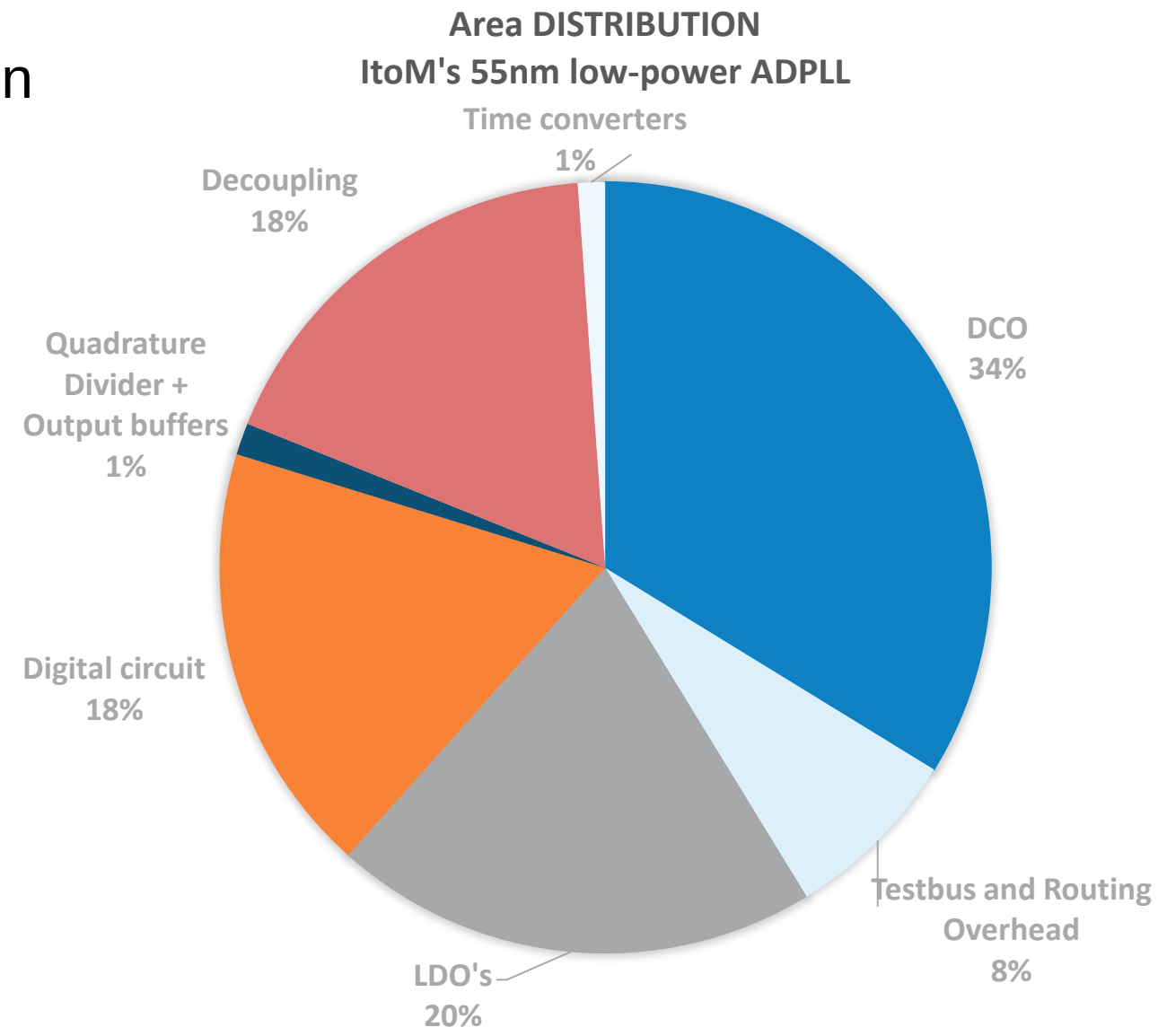
**Low current Medium-performance ADPLL**

- In development in 40nm CMOS

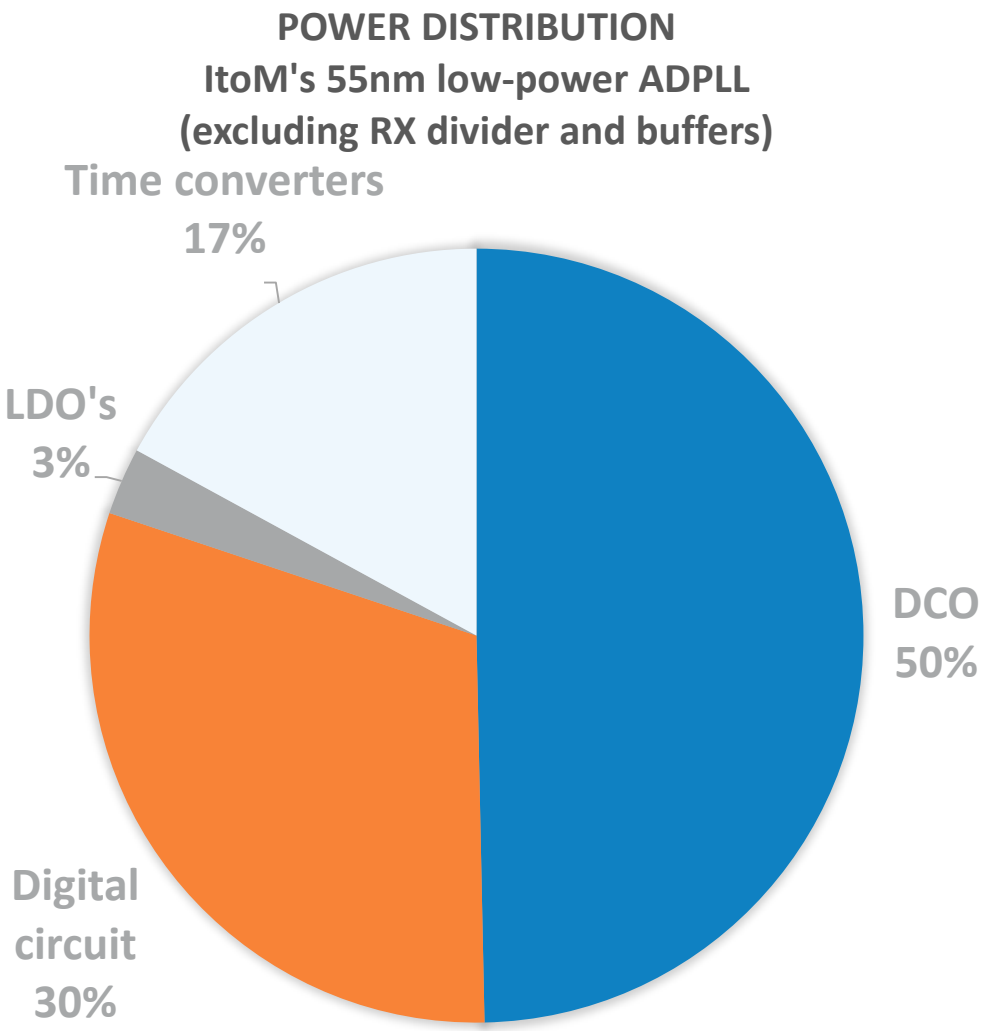
# Design Challenge | Requirement Definition

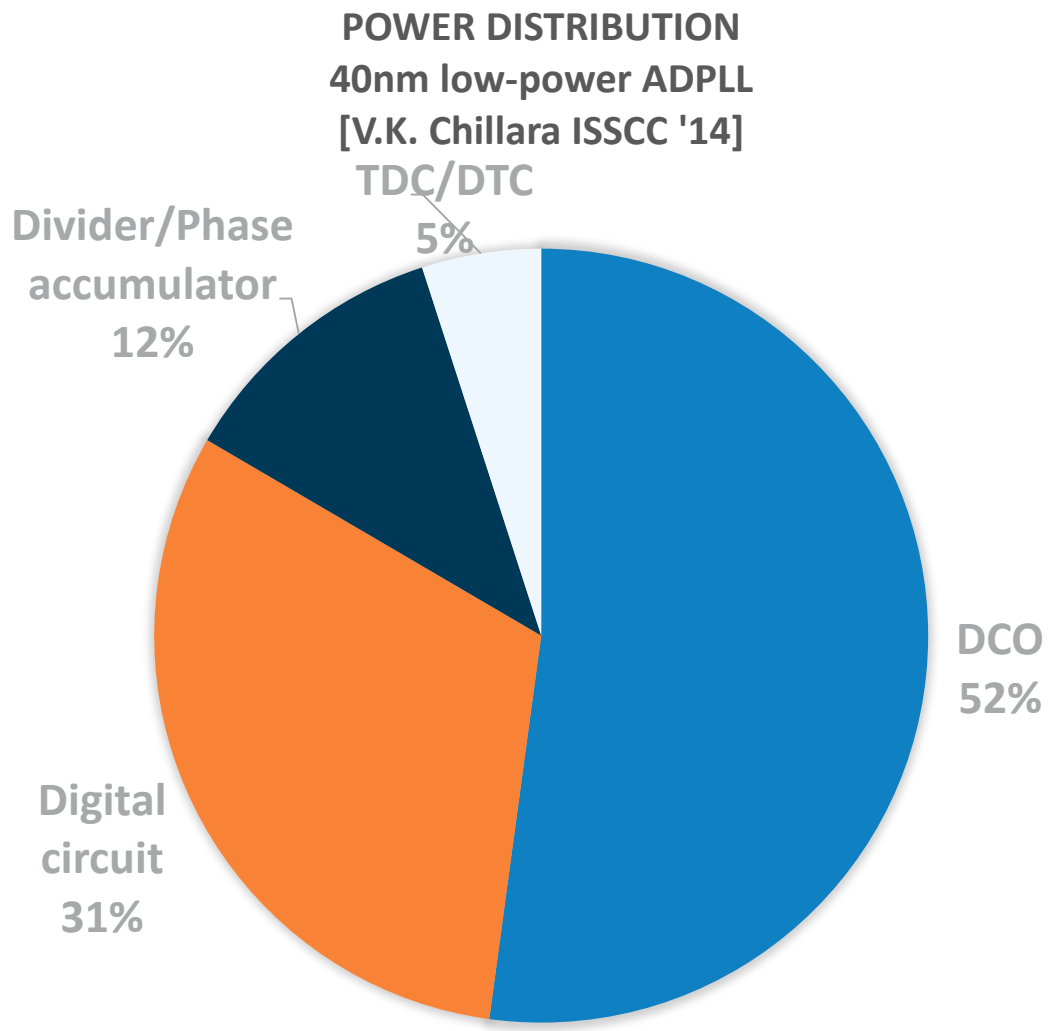
For IoT RF Transceivers the main design objective is to meet the application requirements while minimizing:

- Cost (die area)
- Power consumption

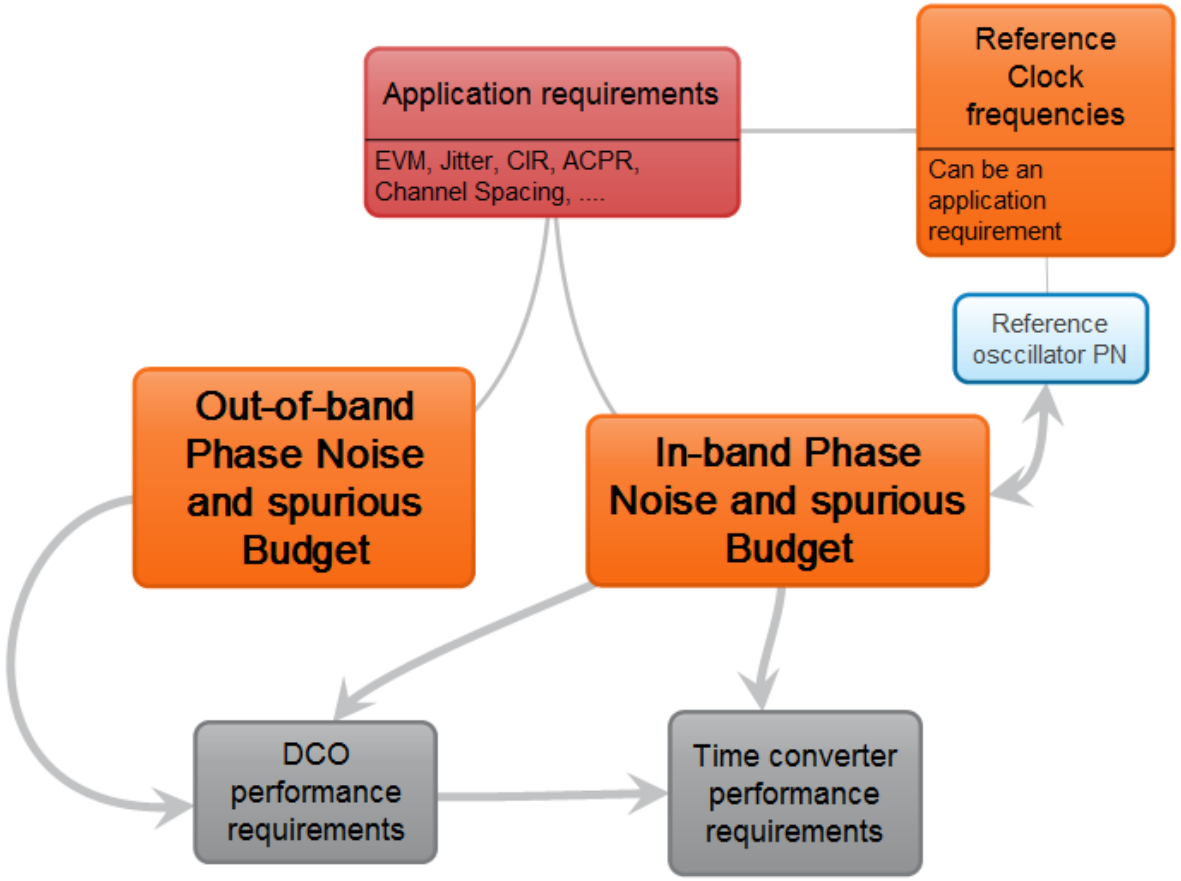


# Design Challenge | Requirement Definition

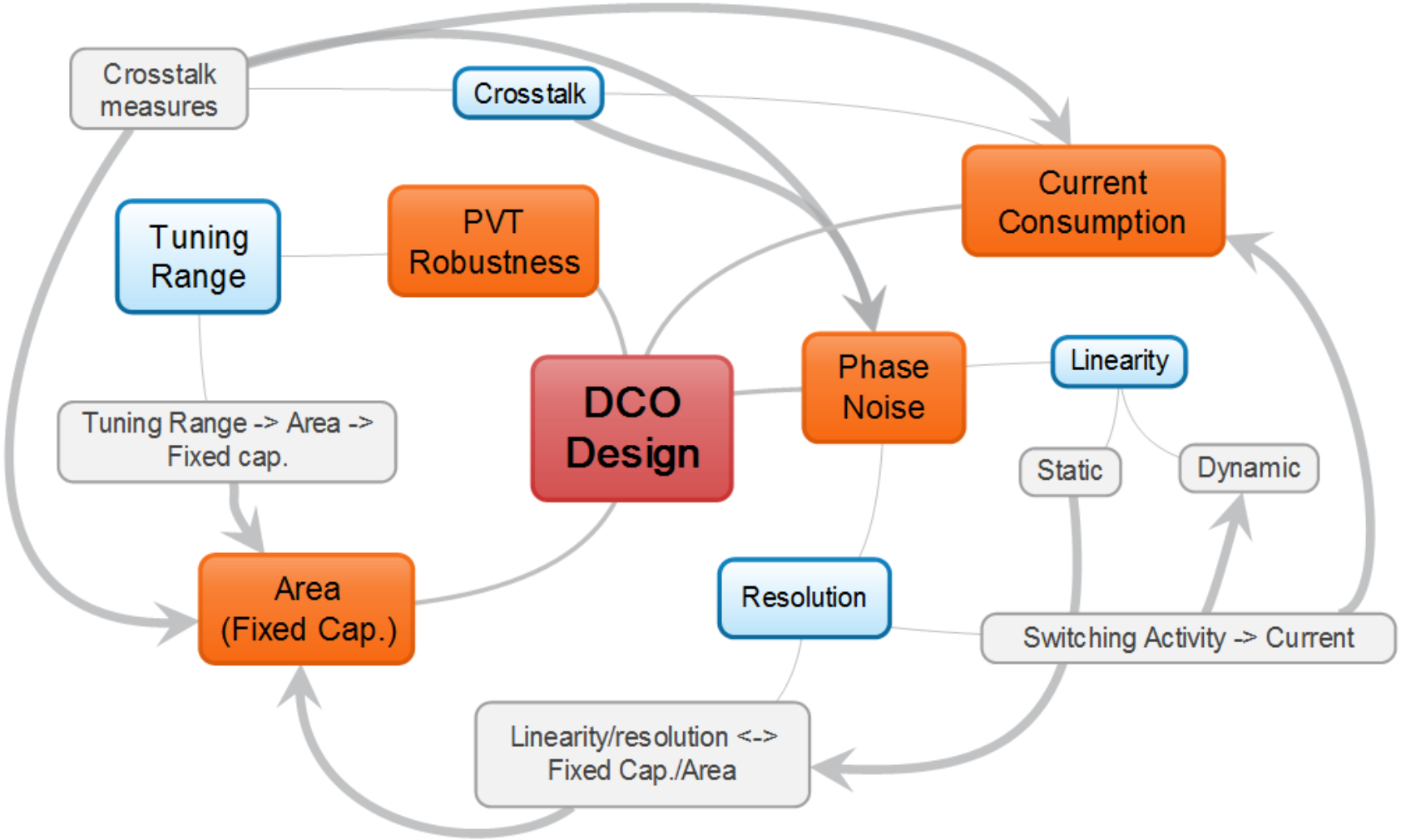


# Design Challenge | Requirement definition



# Design Challenge | DCO design



# Design Challenge | Time converters

**Challenge trade-off between:**

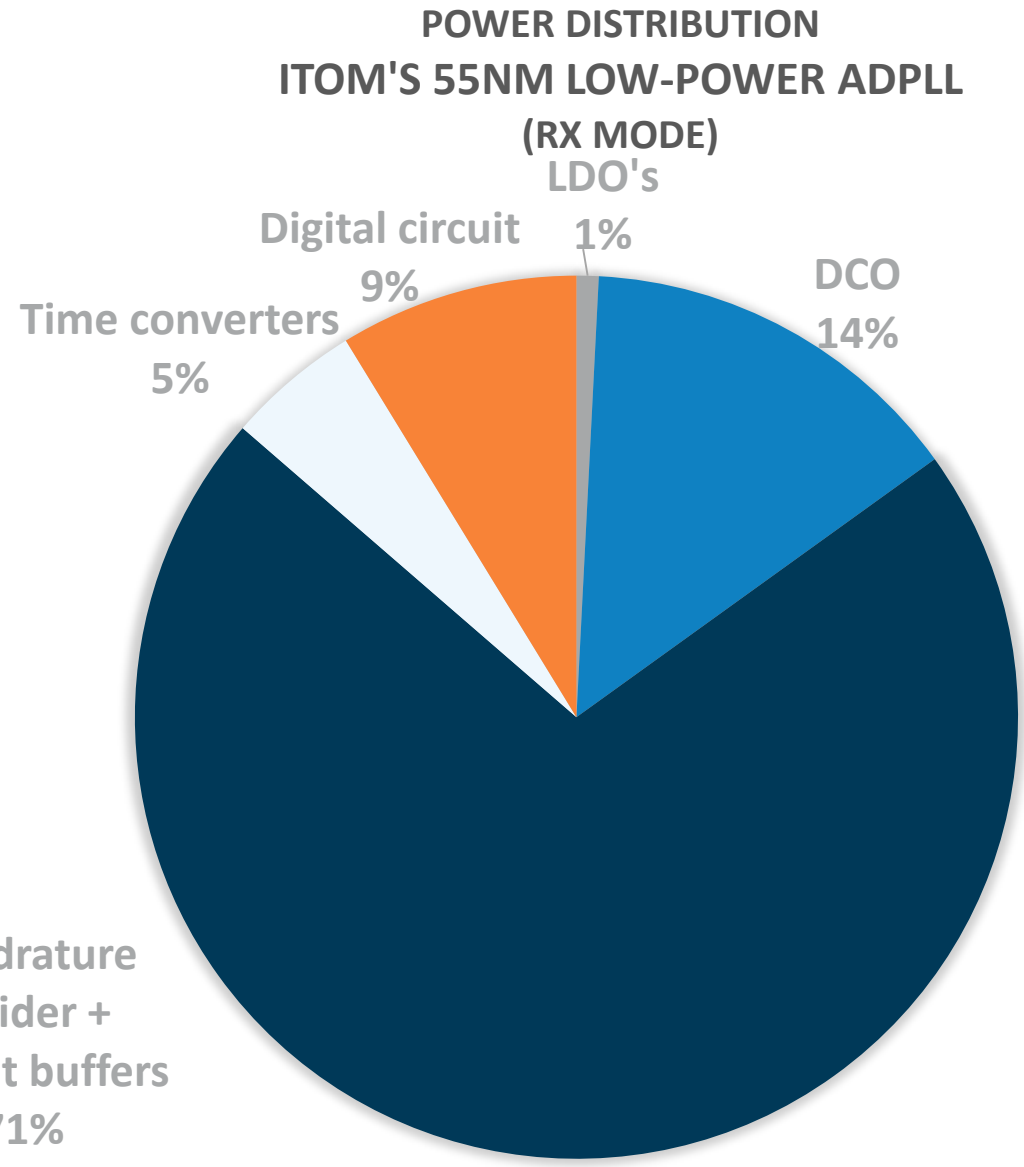
- Resolution
- Linearity
- Range
- Power

**Careful design a “simple” logic gate like structure can already yield acceptable TDC performance:**

- Asymmetrical design
- By using cross coupling, the delay is reduced to one inverter delay rather than one buffer delay

# Design Challenge | Integration

- Power is saved by careful floor-planning this goes beyond the border of the ADPLL IP
- Proper integration is also key meeting other performance requirements

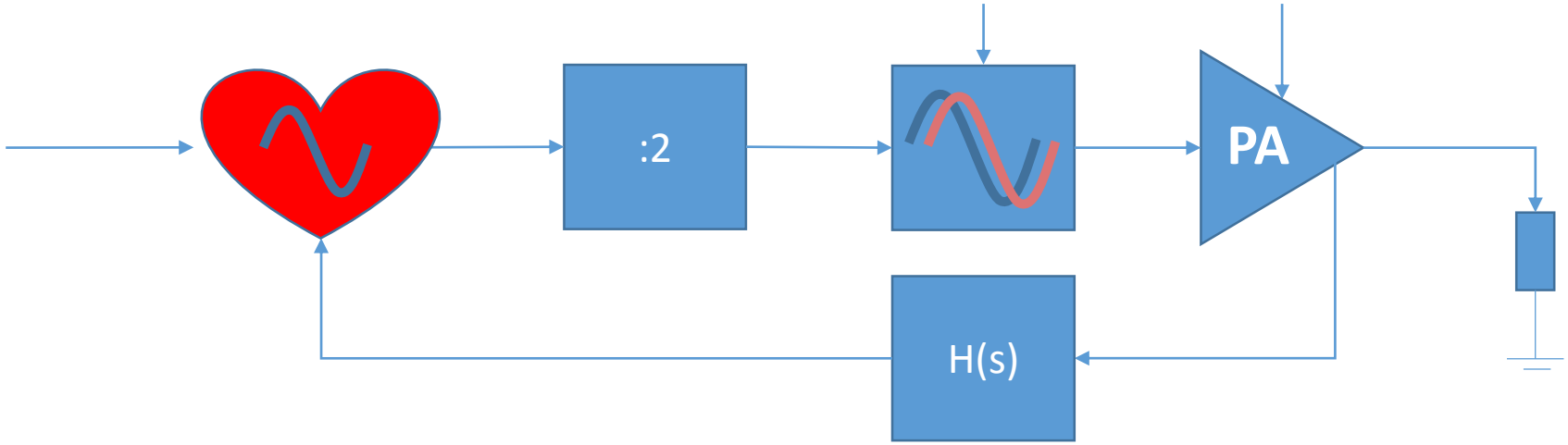


# Opportunities

**The interfaces and observation points are implemented in the digital domain resulting in:**

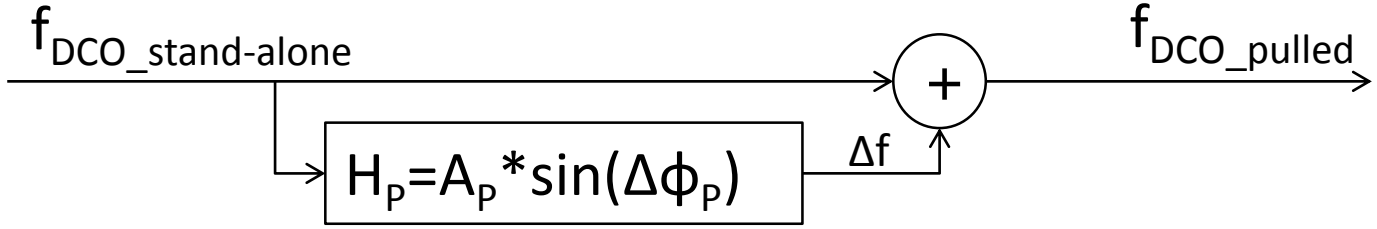
- Getting the most out of the real estate already present
- Large autonomy during factory calibration and test (at negligible area expense)
  - During factory test the tester applies a reference clock, applies some DC voltages and controls a few digital signals while testing:
    - Stuck-at and transition test (Over-speed) of the digital core
    - Stuck-at test of all the interfaces between analog and digital
    - Time converter and DCO linearity (Measurement/Approximation)
    - Modulation quality, Settling time, Drift,
    - …
  - Better portability of the implemented test vectors (Re-use)
- Mitigation options
  - e.g. DCO frequency pulling mitigation

# Opportunities | Frequency pulling Mitigation

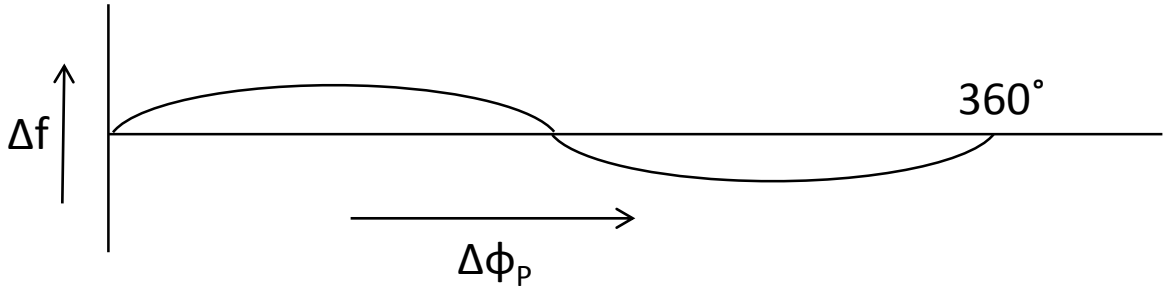



- This concept is known from research [Bashir, JSSC 2011]

# Opportunities | Frequency pulling Mitigation
# Simplified pulling model

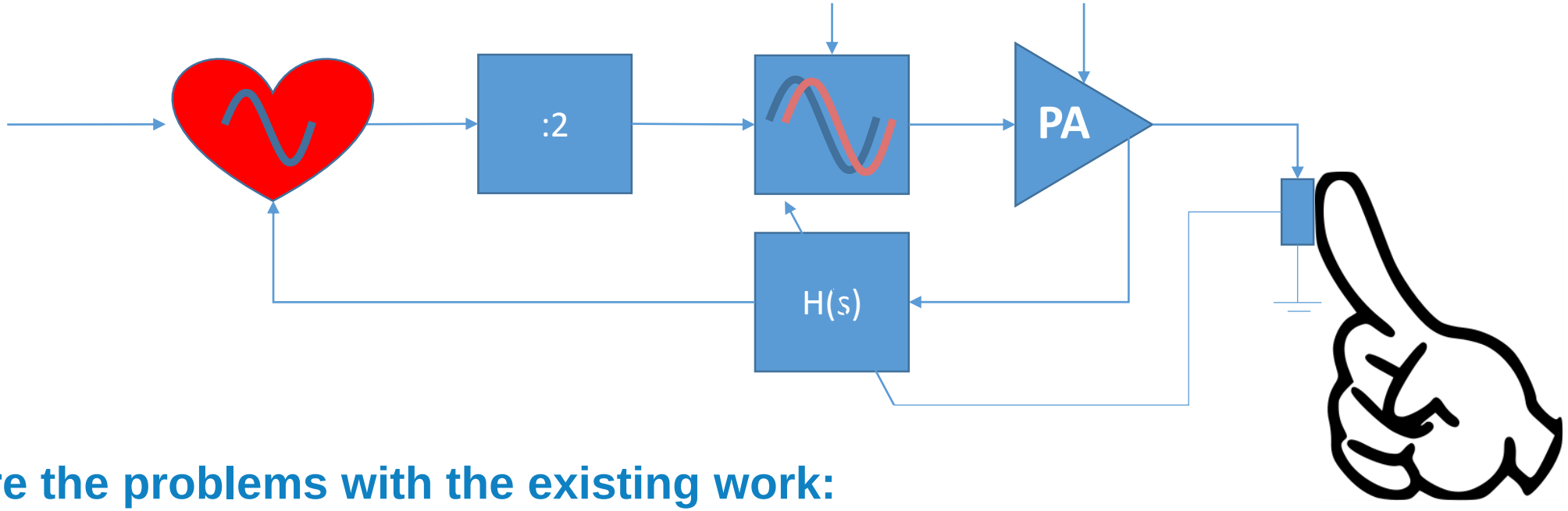



- Pulling magnitude is proportional to $A_P$
  - $A_P$ includes transfer of feedback path
- Pulling can be up or down; periodic function of phase shift in feedback path $\Delta\varphi_P$:




- [A study of locking phenomena in oscillators, Adler, 1946]

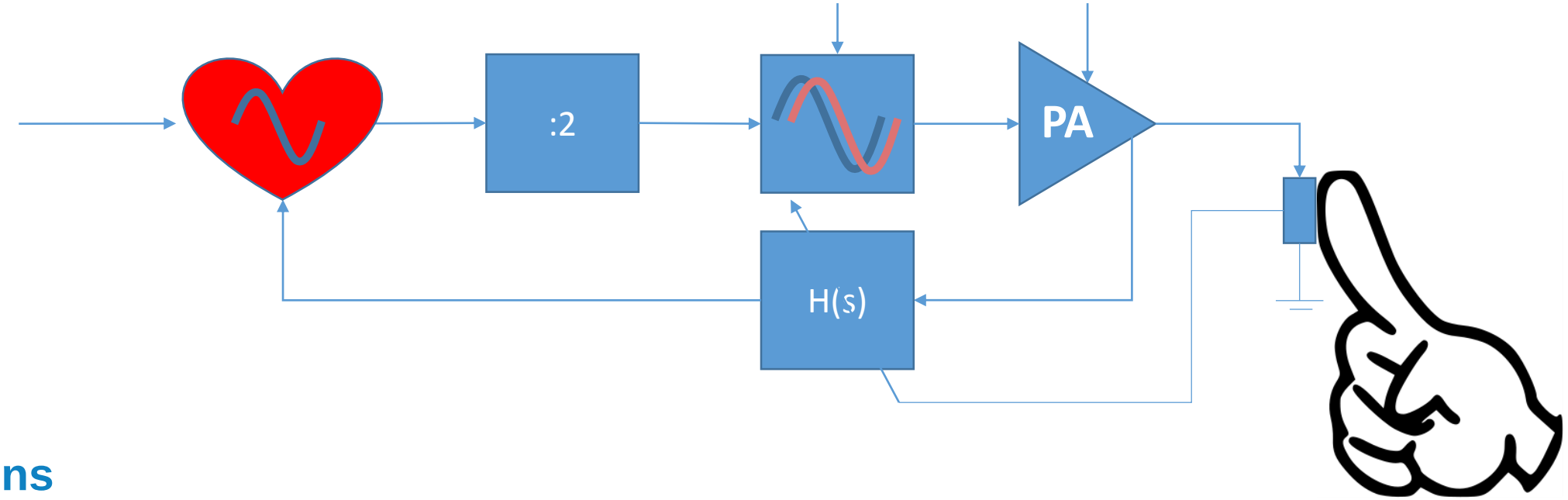
# Opportunities | Frequency pulling Mitigation




## What are the problems with the existing work:

- In a practical application the load changes and therefore the pulling changes over time
  - Due to change in the PA amplitude mostly the amplitude of the pulling changes (Not necessarily a given fact).
    - If the phase is set perfectly this is not an issue (sin(0) = 0)
  - More important due to changes in load both the phase and the amplitude change over time

# Opportunities | Frequency pulling Mitigation



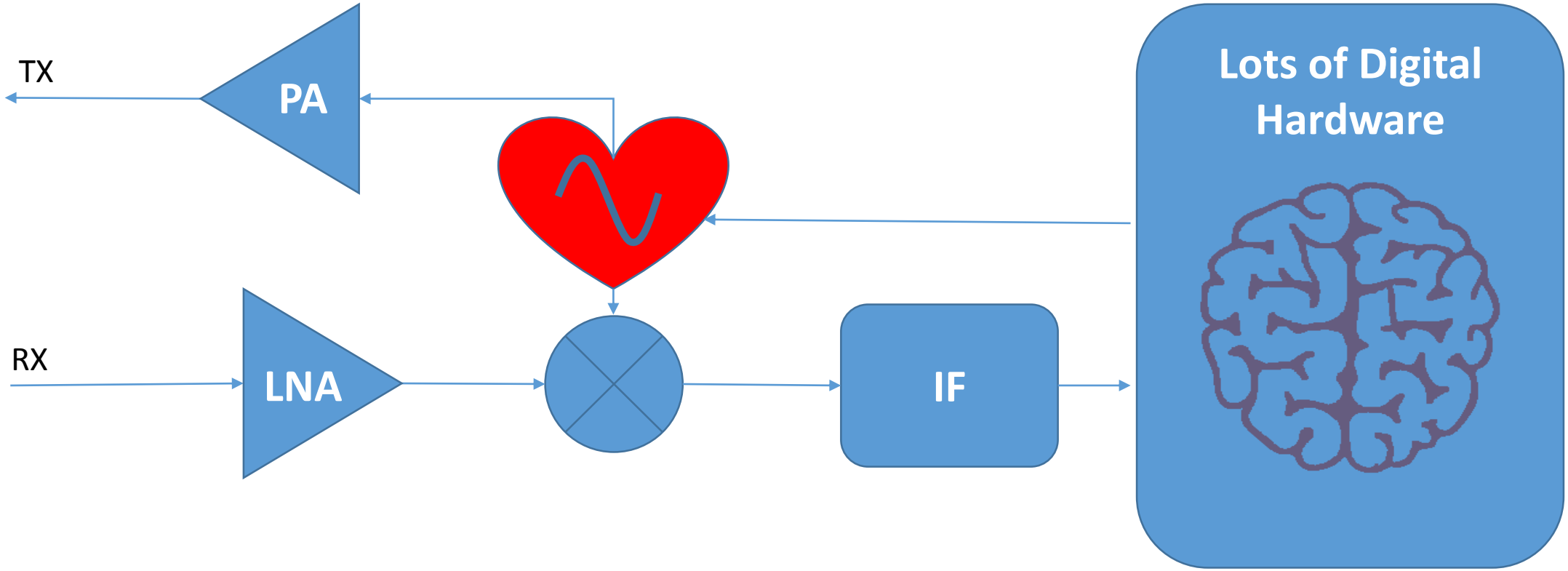

## Solutions

1. Minimize H(s)
   - Proper floor-planning and integration
   - Architectural solution (e.g. Different division ratio)
   - …
2. Increase PLL loop bandwidth
3. An on-line algorithm (control loop)
   - Minimize the correlation between the amplitude modulation and the phase detector code by controlling the phase of the pulling.

# Beyond the next RF Transceiver Generations

- Many application require more than what is offered in SoC on the market:
  - Microcontroller Processing Power
  - Digital Signal Processing functions
  - Sensor interfaces
  - ….
- Increasing digital design complexity
  - Smaller process nodes selected
  - Increasing advantage of ADPLL topology

# Beyond the next RF Transceiver Generations



# Beyond the next RF Transceiver Generations

**Low current Medium-performance ADPLL**

- In development in 40nm CMOS

**High performance ADPLLs for non-transceiver applications**

- Targeting 100fs Jitter performance (a big stable heart)

**Low current ADPLL for IoT applications**

- Sub 40nm CMOS

# Questions?

# References


1. An 860 µW 2.1-2.7 GHz All-digital PLL-based Frequency Modulator with a DTC-assisted Snapshot TDC for WPAN (Bluetooth Smart and ZigBee) Applications, V.K. Chillara, ISSCC-2014
2. A Fully Integrated 28nm Bluetooth Low Energy Transmitter with 36% System Efficiency at 3 dBm, Feng-Wei Kuo, ESSCIRC 2015
3. A study of locking phenomena in oscillators, Adler, 1946
4. A Novel Approach for Mitigation of RF Oscillator Pulling in a Polar Transmitter, Imran Bashir, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 2, FEBRUARY 2011

# Contact Information

**Semiconductor Ideas to the Market (ItoM) B.V.**

Boschdijk 764
5624 CL Eindhoven
The Netherlands

Capitool 10
7521 PL Enschede
The Netherlands

**P** +31 40 2480 604
**F** +31 40 2482 673

**E** info@itom.nl
**I** www.itom.nl